Notice of Allowability	Application No.	Applicant(s)	
	10/725,519	YAMAJI, TAKAFUMI	
	Examiner	Art Unit	
	Richard Chan	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/08/06*.

2. ☒ The allowed claim(s) is/are *3-10 and 12-17*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINERS AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Weyne Tan (Registration No. 55,662) on 1/23/07.

The application has been amended as follows:

17. (Examiner Amended) A radio receiver comprising:

a high frequency filter to filter a receive signal;

a low noise amplifier circuit to amplify the filtered receive signal;

a frequency converter to convert the filtered receive signal into an intermediate frequency signal;

an intermediate filter to filter the intermediate frequency signal;

a variable gain amplifier to amplify the filtered intermediate frequency signal;

a frequency converter to convert the amplified intermediate frequency signal into a low frequency signal; and

a variable resolution analog-to-digital circuit comprising:

a sample-and-hold circuit including a plurality of sample-and-hold units connected in parallel and selectively activated corresponding to a required resoloution to sample and hold an analog input signal;

a plurality of first conversion stages connected in cascade to an output of the sample-and-hold circuit, each of the first conversion stages including a first sub-analog-to-digital converter unit configured to convert a first analog signal to a first digital signal and a plurality of first sub-multiplying-digital-to-analog converter units connected in parallel and selectively activated according to the required resolution to convert the first analog signal and the second analog signal and multiply the first difference signal by a given value, the first analog signal being an analog signal corresponding to the analog input signal;

a plurality of second conversion stages connected in cascade to an output of a last one of the first conversion stages, each of the second conversion stages including a second sub-analog-to-digital convert unit configured to convert a third analog signal into a second digital signal and a second sub-digital-to-analog converter unit to convert the second digital signal into a fourth analog signal and output a second difference signal between the third analog signal and the fourth analog signal; the third analog signal being an analog signal corresponding to the analog input signal; and

a synthesis circuit to synthesize the first digital signal output from each other the first conversion stages and the second digital signal output from each of the second conversion stages, to generate a digital output signal.

Allowable Subject Matter

The following is an examiner's statement of reasons for allowance:

2. Claims 3 – 10, and 12-17 are allowed.

3. The following is an examiner's statement of reasons for allowance:

With respect to claim 3, Yoshioka disclose the variable resolution analog-to-digital converter comprising: a sample-and-hold circuit **Fig.2 circuit 3** including a plurality of sample-and-hold units **3** connected in parallel and selectively activated corresponding to a required resolution to sample and hold an analog input signal; a plurality of first conversion stages **5** connected in cascade to an output of the sample-and-hold circuit, each of the first conversion stages **5** including a first sub-analog-to-digital converter unit **4** configured to convert a first analog signal to a first digital signal and a plurality of first sub-multiplying-digital-to-analog converter units connected in parallel and selectively activated according to the required resolution to convert the first digital signal to a second analog signal, the Velazquez reference than discloses the process of generate a first difference signal between the first analog signal and the second analog signal and multiply the first difference signal by a given value, the first analog signal being an analog signal corresponding to the analog input signal.

However the prior art does not disclose specifically a plurality of second conversion stages connected in cascade to an output of a last one of the first conversion stages, each of the second conversion stages including a second sub-analog-to-digital converter unit configured to convert a third analog signal into a second digital signal and a second sub-digital-to-analog converter unit to convert the second digital signal into a fourth analog signal and output a second difference signal between the third analog signal and the fourth analog signal, the third analog signal being an analog signal corresponding to the analog input signal; and a synthesis circuit to synthesize the first digital signal output from each of the first conversion stages and the second digital signal output from each of the second conversion stages, to generate a digital output signal.

Claims 4-10 are dependent on allowable claim 3.

With respect to claim 12, Yoshioka discloses the variable resolution analog-to-digital converter comprising: a sample-and-hold circuit **Fig.2 circuit 3**including a plurality of sample-and-hold units **circuit 3** which are connected in parallel and selectively used corresponding to a required resolution to sample and hold an analog input signal; a plurality of conversion stages **conversion stages 5** connected in cascade to an output of the sample-and-hold circuit **3**, each of the conversion stages including a sub-analog-to-digital converter unit **4** configured to convert a first analog signal into a digital signal and a switch **7** which turns on or off according to the required

resolution to bypass at least an initial stage of the conversion stages; and a synthesis circuit **6** configured to synthesize digital signals each provided by each of the conversion stages, to generate a digital output signal, however Yoshioka does not specifically disclose a sub-digital-to-analog converter unit to convert the digital signal into a second analog signal and output a difference signal between the first analog signal and the second analog signal, the first analog signal being an analog signal corresponding to the analog input signal.

The Velazquez reference (US 5,568,142) however discloses in Fig.6 digital-to-analog converter units **62** to convert the digital signal into a second analog signal and output a difference signal between the first analog signal and the second analog signal, the first analog signal being an analog signal corresponding to the analog input signal; **(Col.11 lines 10-31)**,

However the prior art does not disclose the converter further includes a clock phase inverting circuit configured to invert, when the switch turns on, a phase of a clock signal supplied to the conversion stages except for at least the initial one of the conversion stages with respect to a phase of the clock signal when the switch turns off.

With respect to claim 13, Yoshioka discloses the variable resolution analog-to-digital converter comprising: a sample-and-hold circuit **3** including a plurality of sample-and-hold units **3** which are connected in parallel and selectively used according to a required resolution to sample and hold an analog input signal; a plurality of unit delay circuits **1806** connected in cascade to delay an output signal from the sample-and-hold

circuit; **(Paragraph 0021]** an analog linear transformation circuit to subject a set of output signals from the unit delay circuits to a first linear transformation to output a plurality of linear transformed analog signal; a plurality of sub-analog-to-digital converter units **4** to convert the linear transformed analog signal into a plurality of digital signals.

However the prior art does not disclose wherein a digital linear transformation circuit to subject a set of digital signals of the digital signals output from the sub-analog-to-digital converter units to a second linear conversion that is an inverting transformation of the first linear transform, to output a plurality of digital signals output by the sub-analog-to-digitals; and a digital delay adder circuit to add the linear digital signals with the same delay time as that of the analog delay circuit to generate a digital output signal.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard Chan whose telephone number is (571) 272-0570. The examiner can normally be reached on Mon - Fri (9AM - 5PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nay Maung can be reached on (571)272-7882. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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1/23/07

NAY MAUNG
SUPERVISORY PATENT EXAMINER